Freescale Semiconductor
Technical Data

Document Number: MRF8P23080H
Rev. 1, 11/2010

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

MRF8P23080HR3
MRF8P23080HSR3

2300-2400 MHz, 16 W AVG., 28 V
W-CDMA, LTE
LATERAL N-CHANNEL
RF POWER MOSFETs

Designed for W-CDMA and LTE base station applications with frequencies from 2300 to 2620 MHz. Can be used in Class AB and Class C for all typical cellular base station modulation formats.

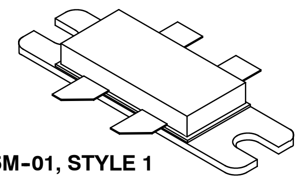
- Typical Doherty Single-Carrier W-CDMA Performance: V_{DD} = 28 Volts, I_{DQA} = 280 mA, V_{GSB} = 0.7 Vdc, P_{out} = 16 Watts Avg., IQ Magnitude Clipping, Channel Bandwidth = 3.84 MHz, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF.

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
2300 MHz	14.6	42.0	6.7	-29.5
2350 MHz	14.7	41.6	6.8	-31.5
2400 MHz	14.6	41.4	6.6	-32.5

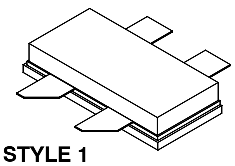
- Capable of Handling 10:1 VSWR, @ 32 Vdc, 2350 MHz, 90 Watts CW Output Power (3 dB Input Overdrive from Rated P_{out})
- Typical P_{out} @ 3 dB Compression Point ≃ 100 Watts CW

Features

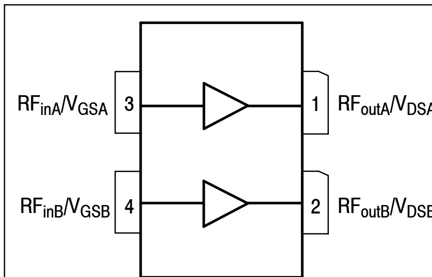
- Production Tested in a Symmetrical Doherty Configuration
- 100% PAR Tested for Guaranteed Output Power Capability
- Characterized with Large-Signal Load-Pull Parameters and Common Source S-Parameters
- Internally Matched for Ease of Use
- Integrated ESD Protection
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction Systems
- RoHS Compliant
- NI-780-4 in Tape and Reel. R3 Suffix = 250 Units, 56 mm Tape Width, 13 inch Reel.
- NI-780S-4 in Tape and Reel. R3 Suffix = 250 Units, 32 mm Tape Width, 13 inch Reel.



CASE 465M-01, STYLE 1
NI-780-4
MRF8P23080HR3



CASE 465H-02, STYLE 1
NI-780S-4
MRF8P23080HSR3



(Top View)

Figure 1. Pin Connections

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature (1,2)	T_J	225	°C
CW Operation @ T_C = 25°C Derate above 25°C	CW	168 2.39	W W/°C

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

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Table 2. Thermal Characteristics

Characteristic	Symbol	Value (1,2)	Unit
Thermal Resistance, Junction to Case Case Temperature 72°C, 16 W CW, 28 Vdc, I_{DQA} = 280 mA, V_{GSB} = 0.7 V, 2300 MHz Case Temperature 80°C, 80 W CW(3), 28 Vdc, I_{DQA} = 280 mA, V_{GSB} = 0.7 V, 2300 MHz	$R_{\theta JC}$	 0.89 0.55	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2 (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	IV (Minimum)

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics (4)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics (4)					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 75 μAdc)	$V_{GS(th)}$	1.0	1.8	2.5	Vdc
Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_{DA} = 280 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	1.9	2.6	3.4	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 0.75 Adc)	$V_{DS(on)}$	0.1	0.23	0.3	Vdc

Functional Tests (5,6) (In Freescale Doherty Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQA} = 280 mA, V_{GSB} = 0.7 Vdc, P_{out} = 16 W Avg., f = 2300 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured on 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.

Characteristic	Symbol	Min	Typ	Max	Unit
Power Gain	G_{ps}	13.5	14.6	18.5	dB
Drain Efficiency	η_D	38.0	42.0	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	6.0	6.7	—	dB
Adjacent Channel Power Ratio	ACPR	—	-29.5	-27.0	dBc

Typical Broadband Performance (6) (In Freescale Doherty Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQA} = 280 mA, V_{GSB} = 0.7 Vdc, P_{out} = 16 W Avg., Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
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1. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
2. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.
3. Exceeds recommended operating conditions. See CW operation data in Maximum Ratings table.
4. Each side of device measured separately.
5. Part internally matched both on input and output.
6. Measurement made with device in a Symmetrical Doherty configuration

(continued)

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Typical Performances (1) (In Freescale Doherty Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQA} = 280 mA, V_{GSB} = 0.7 Vdc, 2300–2400 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	55	—	W
P_{out} @ 3 dB Compression Point, CW	P3dB	—	100	—	W
IMD Symmetry @ 20 W PEP, P_{out} where IMD Third Order Intermodulation ≅ 30 dBc (Delta IMD Third Order Intermodulation between Upper and Lower Sidebands > 2 dB)	IMD_{sym}	—	30	—	MHz
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	55	—	MHz
Gain Flatness in 100 MHz Bandwidth @ P_{out} = 16 W Avg.	G_F	—	0.1	—	dB
Gain Variation over Temperature (–30°C to +85°C)	ΔG	—	0.013	—	dB/°C
Output Power Variation over Temperature (–30°C to +85°C) (2)	ΔP1dB	—	0.005	—	dB/°C

1. Measurement made with device in a Symmetrical Doherty configuration.
2. Exceeds recommended operating conditions. See CW operation data in Maximum Ratings table.

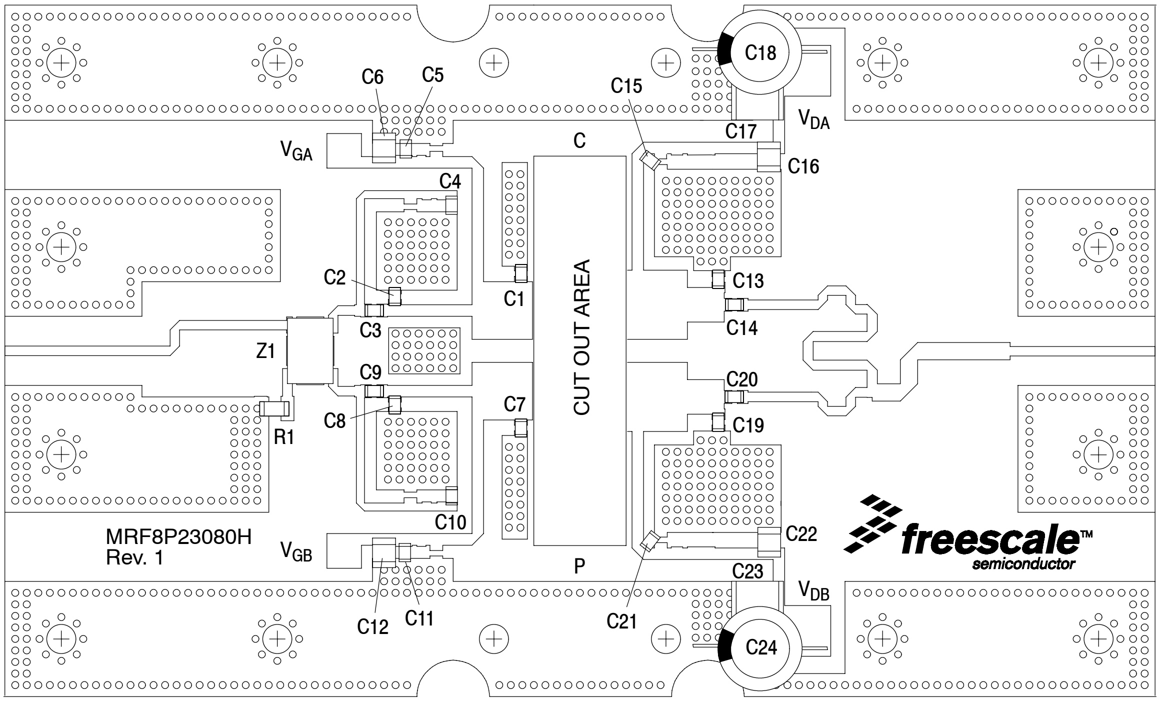


Figure 2. MRF8P23080HR3(HSR3) Test Circuit Component Layout

Table 5. MRF8P23080HR3(HSR3) Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C7	0.8 pF Chip Capacitors	ATC600F0R8JT250XT	ATC
C2, C8, C13, C19	1.0 pF Chip Capacitors	ATC600F1R0JT250XT	ATC
C3, C9	18 pF Chip Capacitors	ATC600F180JT250XT	ATC
C4, C5, C10, C11	8.2 pF Chip Capacitors	ATC600F8R2JT250XT	ATC
C6, C12, C16, C22	1.0 μF, 50 V Chip Capacitors	GRM21BR71H105KA12L	Murata
C14, C20	10 pF Chip Capacitors	ATC600F100JT250XT	ATC
C15, C21	5.6 pF Chip Capacitors	ATC600F5R6JT250XT	ATC
C17, C23	10 μF, 50 V Chip Capacitors	GRM55DR61H106KA88L	Murata
C18, C24	470 μF, 63 V Electrolytic Capacitors	MCGPR63V477M13X26-RH	Multicomp
R1	50 Ω, 1/4 W Chip Resistor	CRCW120650R0FKEA	Vishay
Z1	2500 MHz Band 90°, 3 dB Chip Hybrid Coupler	GSC356-HYB2500	Soshin
PCB	0.020″, ε_r = 3.5	RO4350B	Rogers

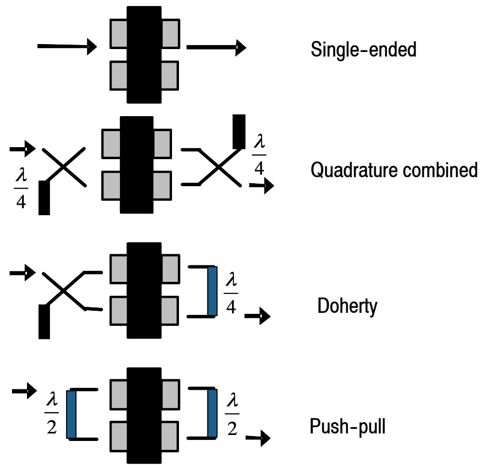


Figure 3. Possible Circuit Topologies

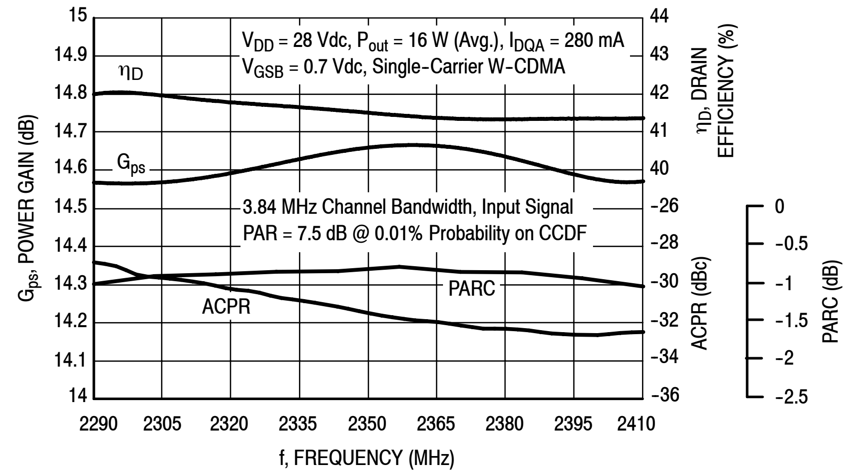


Figure 4. Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 16 Watts Avg.

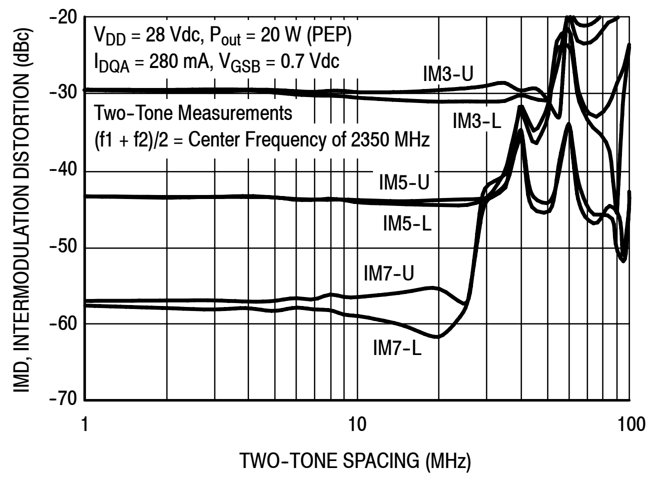


Figure 5. Intermodulation Distortion Products versus Two-Tone Spacing

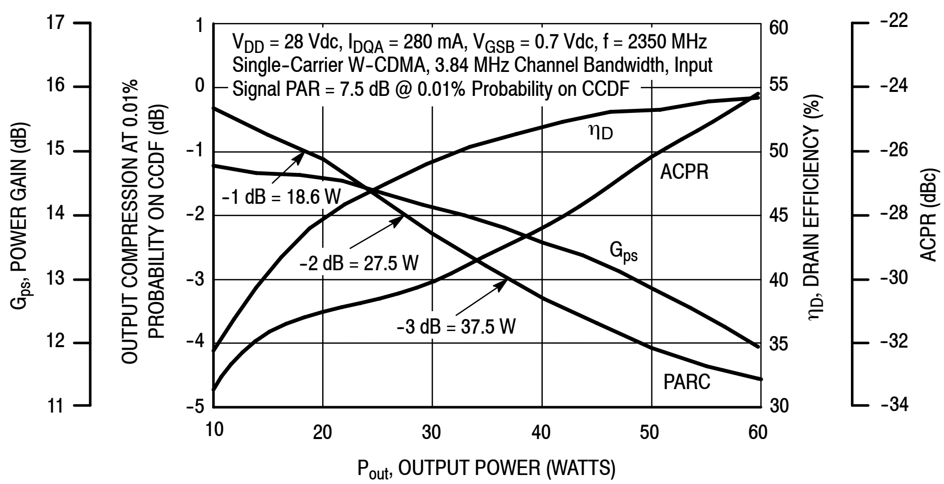


Figure 6. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS

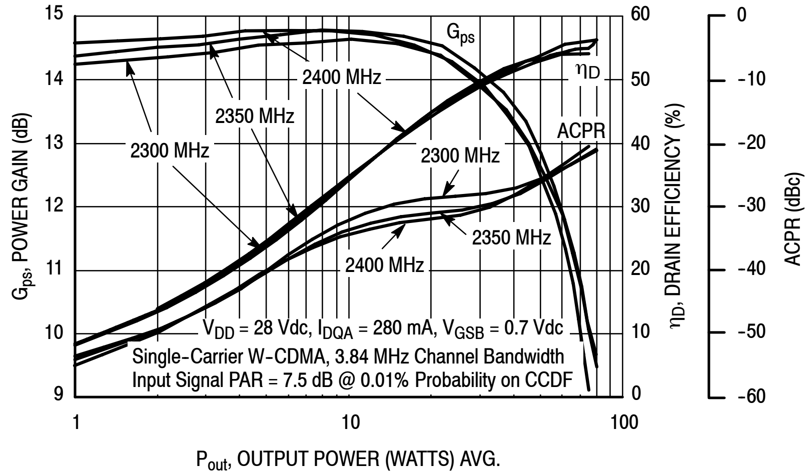


Figure 7. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

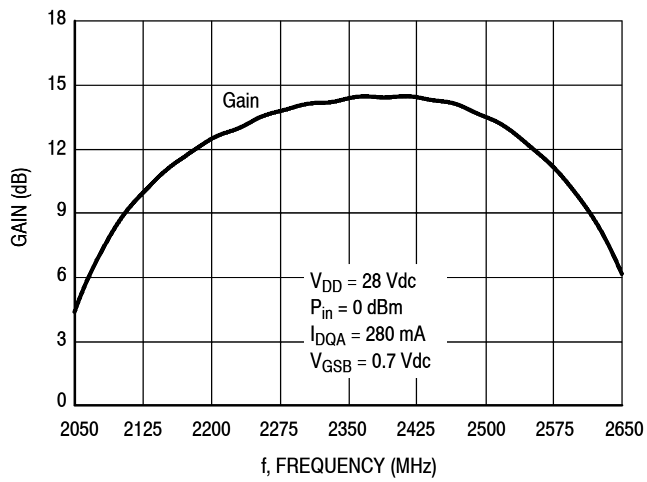


Figure 8. Broadband Frequency Response

W-CDMA TEST SIGNAL

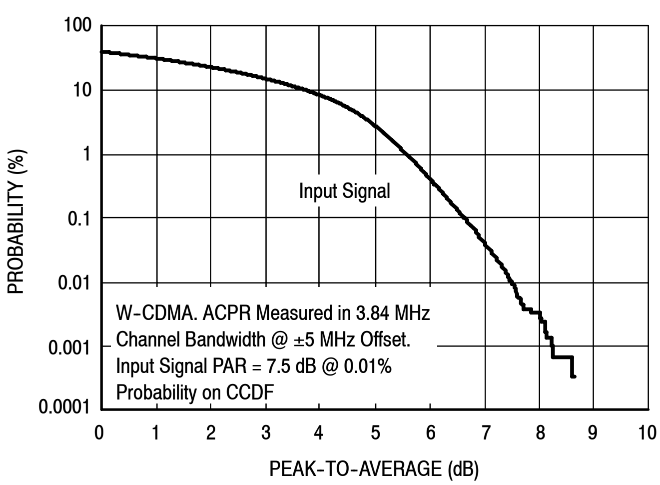


Figure 9. CCDF W-CDMA IQ Magnitude Clipping, Single-Carrier Test Signal

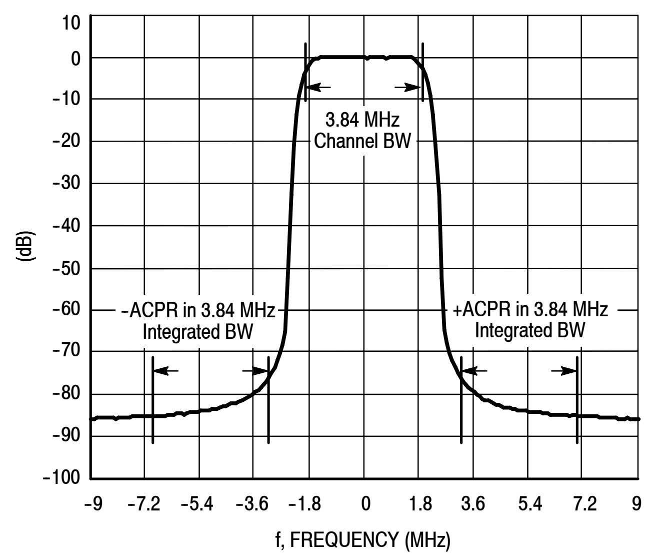


Figure 10. Single-Carrier W-CDMA Spectrum

V_{DD} = 28 Vdc, I_{DQA} = 280 mA

f MHz	Max P_{out} (1)		Z_{source} Ω	Z_{load} Ω
	Watts	dBm		
2300	58	47.6	8.42 - j14.3	3.51 - j5.02
2350	55	47.4	11.4 - j13.4	3.75 - j5.03
2400	55	47.4	17.7 - j9.34	3.14 - j5.63

(1) Maximum output power measurement reflects pulsed 1 dB gain compression.

Z_{source} = Test circuit impedance as measured from gate contact to ground.

Z_{load} = Test circuit impedance as measured from drain contact to ground.

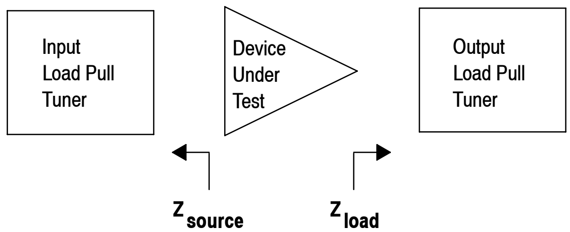


Figure 11. Carrier Side Load Pull Performance — Maximum P1dB Tuning

V_{DD} = 28 Vdc, I_{DQA} = 280 mA

f MHz	Max Eff. (1) %	Z_{source} Ω	Z_{load} Ω
2300	60.9	8.41 - j14.3	7.02 - j3.44
2350	60.1	11.4 - j13.4	6.84 - j2.41
2400	60.0	17.7 - j9.35	6.53 - j2.92

(1) Maximum efficiency measurement reflects pulsed 1 dB gain compression.

Z_{source} = Test circuit impedance as measured from gate contact to ground.

Z_{load} = Test circuit impedance as measured from drain contact to ground.

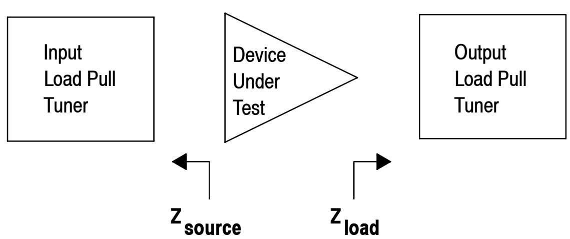
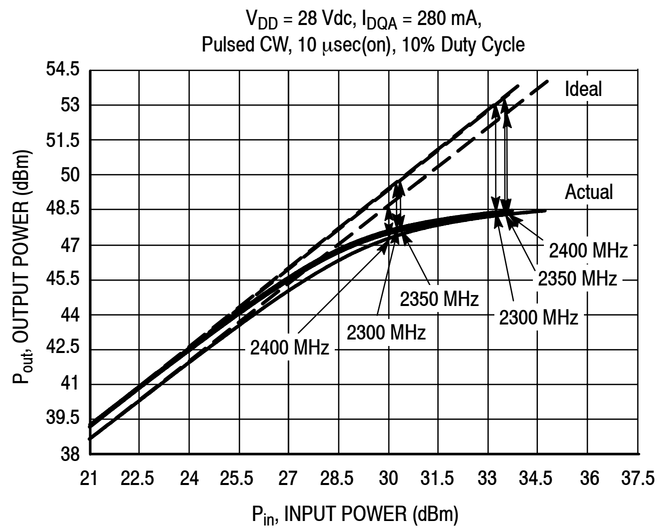


Figure 12. Carrier Side Load Pull Performance — Maximum Efficiency Tuning

ALTERNATIVE PEAK TUNE LOAD PULL CHARACTERISTICS



NOTE: Load Pull Test Fixture Tuned for Peak P1dB Output Power @ 28 V

f (MHz)	P1dB		P3dB	
	Watts	dBm	Watts	dBm
2300	59	47.7	69	48.4
2350	58	47.6	68	48.3
2400	54	47.3	68	48.3

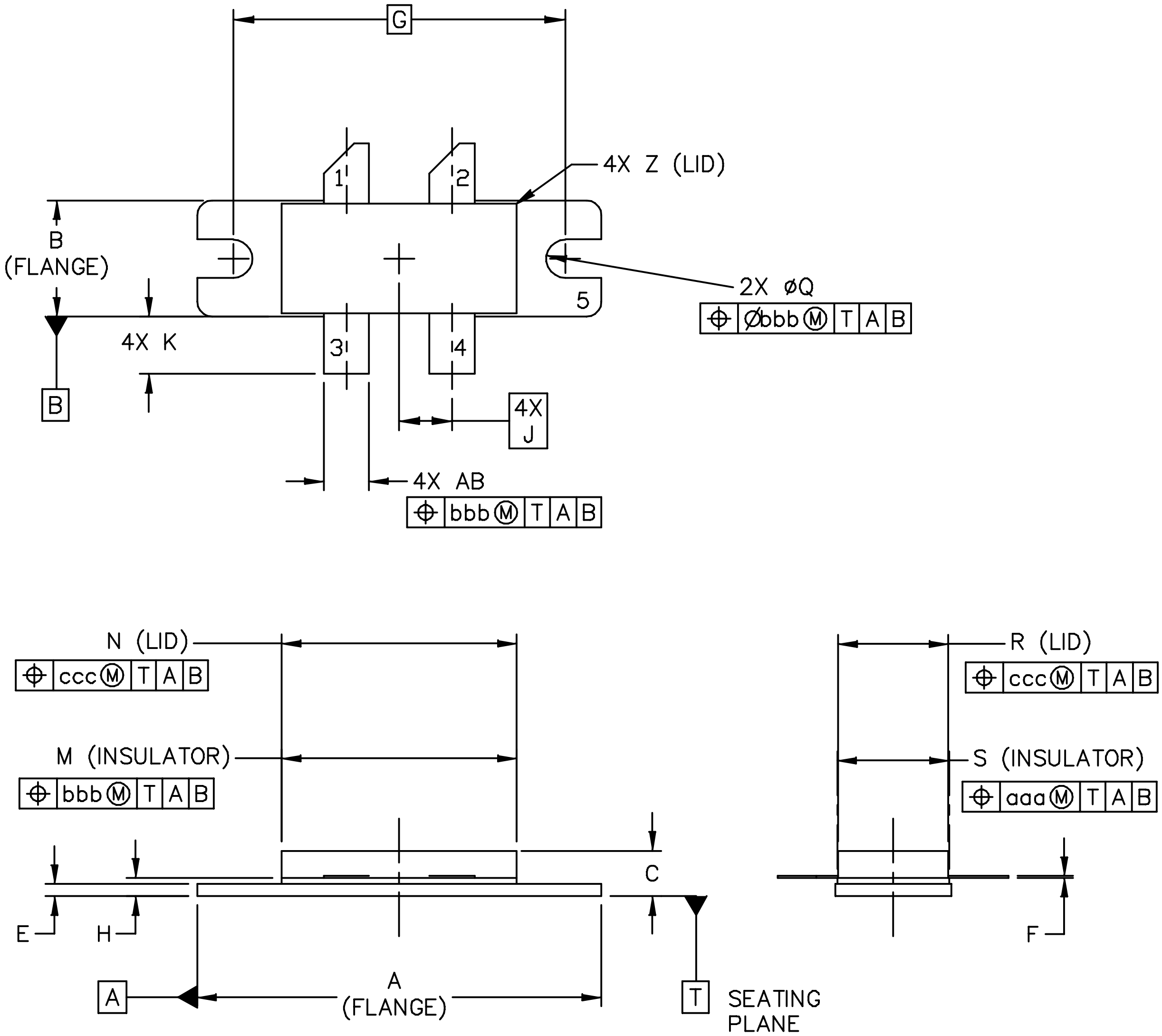
Test Impedances per Compression Level

f (MHz)		Z_{source} Ω	Z_{load} Ω
2300	P1dB	8.40 – j14.3	3.60 – j5.30
2350	P1dB	11.4 – j13.4	3.70 – j5.20
2400	P1dB	17.7 – j9.30	3.10 – j5.10

Figure 11. Pulsed CW Output Power versus Input Power @ 28 V

NOTE: Measurement made on the Class AB, carrier side of the device.

PACKAGE DIMENSIONS



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	CASE NUMBER: 465M-01		27 MAR 2007
	STANDARD: NON-JEDEC		

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.

2. CONTROLLING DIMENSION: INCH.

3. DIMENSION H IS MEASURED .030 (0.762) AWAY FROM PACKAGE BODY.

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. GATE
5. SOURCE

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	1.335	1.345	33.91	34.16	R	.365	.375	9.27	9.53
B	.380	.390	9.65	9.91	S	.365	.375	9.27	9.52
C	.125	.170	3.18	4.32	U		.040		1.02
E	.035	.045	0.89	1.14	Z		.030		0.76
F	.003	.006	0.08	0.15	AB	.145	.155	3.68	3.94
G	1.100 BSC		27.94 BSC						
H	.057	.067	1.45	1.7	aaa	.005		0.127	
J	.175 BSC		4.44 BSC		bbb	.010		0.254	
K	.170	.210	4.32	5.33	ccc	.015		0.381	
M	.774	.786	19.61	20.02					
N	.772	.788	19.61	20.02					
Q	ø.118	ø.138	ø3	ø3.51					

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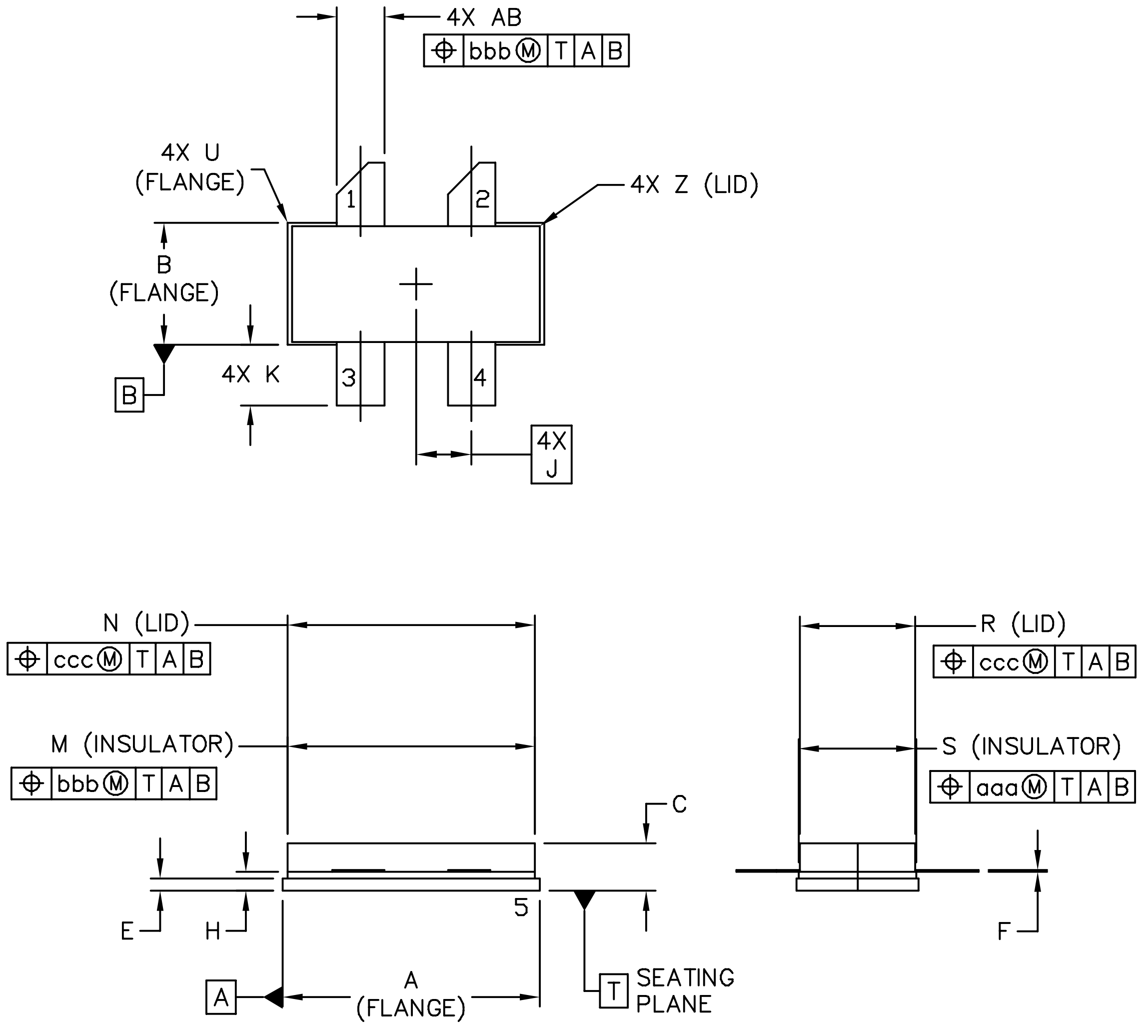

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STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. GATE
5. SOURCE

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
A	.805	.815	20.45	20.7	U		.040		1.02
B	.380	.390	9.65	9.91	Z		.030		0.76
C	.125	.170	3.18	4.32	AB	.145	.155	3.68	3.94
E	.035	.045	0.89	1.14					
F	.003	.006	0.08	0.15	aaa	.005		0.127	
H	.057	.067	1.45	1.7	bbb	.010		0.254	
J	.175 BSC		4.44 BSC		ccc	.015		0.381	
K	.170	.210	4.32	5.33					
M	.774	.786	19.61	20.02					
N	.772	.788	19.61	20.02					
R	.365	.375	9.27	9.53					
S	.365	.375	9.27	9.52					

MECHANICAL OUTLINE

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PRODUCT DOCUMENTATION AND SOFTWARE

Refer to the following documents and software to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

For Software, do a Part Number search at http://www.freescale.com, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	May 2010	• Initial Release of Data Sheet
1	Nov. 2010	• Updated frequency in overview paragraph from “2300 to 2400 MHz” to “2300 to 2620 MHz” to show the broadband performance of the part, p. 1 • In Table 2, Thermal Characteristics, P_{out} = 16 W CW thermal resistance value changed from 0.91 to 0.89°C/W and P_{out} = 80 W CW thermal resistance value changed from 0.91 to 0.55°C/W. Thermal values now reflect the use of the combined dissipated power from the carrier amplifier and peaking amplifier, p. 2. • Broadband IRL data removed from Fig. 4, Output Peak-to-Average Ratio Compression (PARC) Broadband Performance and Fig. 8, Broadband Frequency Response graphs. Data not valid indicator of product performance due to circuit implementation, p. 6, 7.

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